REMARKS

The Examiner is thanked for her careful and very thorough Office Action. The Examiner is particularly thanked for the helpful suggestions regarding correction of the alleged informalities.

Claim 2 has been canceled by a previous amendment. Claims 1 and 3-8 are pending. Claim 6 is allowed. Claims 1, 3-5, 7, and 8 have been rejected. By the foregoing amendments, various Claims are sought to be amended or canceled without prejudice.

Note that the amendments to Claims 1 and 4-8 are intended to be purely formal amendments, and are believed not to change the scope of these claims.

Rejections Under 35 USC 112

The Examiner has rejected Claims 1 and 8 under 35 USC 112, second paragraph. The Examiner has suggested that the limitation of "essentially unique mapped" renders the claims indefinite because it is not clear as to what is being claimed by using this phrase. Applicant respectfully disagrees with this suggestion.

The Examiner has asked what "essentially unique mapped" mean in these claims. Applicant respectfully submits that "essentially unique mapped" refers generally to the fact that:

> **Each texel can ... be uniquely identified by its index and map level or (i, j, map). (page 10, lines 7-8).**

The Examiner has also asked what is mapped to what that is unique. Applicant respectfully submits, again, that each texel is mapped to an index and a map level that uniquely identifies that particular texel.

Finally, the Examiner appears to ask what the cache tag assignment is mapped to. Applicant respectfully submits that the cache tag assignment is mapped to a particular texel.

The Examiner is respectfully reminded that:

> In construing the meaning of a claim limitation, it is entirely proper to look to the specification in order to interpret what the inventor intended by the claim term. *In re Sneed*, 710 F2d. 1544, 1548, 218 U.S.P.Q. 385,

> 388 (Fed. Cir. 1983) ("It is axiomatic that, in proceedings before the PTO, claims in an application are to be given their broadest reasonable interpretation consistent with the specification, . . . , and that claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art."); *In re Marosi*, 710 F.2d 799, 802-03, 218 U.S.P.Q. 289, 292 (Fed. Cir. 1983) ("It is well established that 'claims are not to be read in a vacuum, and limitations therein are to be read in light of the specification . . .'"); *In re Ehrreich*, 590 F.2d 902, 907, 200 U.S.P.Q. 504, 508 (CCPA 1979).

The Examiner has also rejected Claims 1 and 4-8 because some elements recited in these claims have insufficient antecedent basis. By the above amendments, Applicant has amended the claims to correct the alleged informalities. No new matter has been added by the amendments, and all of the Examiner's concerns have been addressed.

Accordingly, Applicant respectfully requests withdrawal of these rejections.

Art Rejections

The art rejections are all respectfully traversed.

Rejection Under 35 USC 102(b)

Claims 1, 3-5, 7, and 8 stand rejected under 35 USC Section 102(b) as anticipated by *Gannett*.

Claim 1

> A graphics processing method, comprising the steps of:
> (a.) caching texture memory fetches, using a cache tag assignment which is essentially unique mapped, said cache tag assignment having a tag length and mip mapping addresses, while
> (b.) generating condensed cache tags, by removing two bits from the tag length by means of a remapping which exploits different address resolutions implied by level of detail settings in different mip mapping processes to re-encode the mip mapping addresses
> (c.) and using said condensed tags for said caching step (a.).

Claim 1 recites features not taught or suggested by *Gannett*. Specifically, Claim 1 recites, "generating condensed cache tags, by removing two bits from the tag length by means of a remapping which exploits different address resolutions implied by level of

detail settings in different mip mapping processes to re-encode the mip mapping addresses."

1. *Gannett* does not teach or suggest the claimed limitation of "generating condensed cache tags", much less by means of a remapping.

Gannett relates to a daemon based virtual memory management of a hardware device local cache memory system that stores texture mapping data. *Gannett* simply discloses a 23-bit tag with:

> *...eight bits representing the texture ID of the texture data, a bit used in determining the map number of the texture data, and the seven high-order S and T coordinates of the texture data.*" (col. 19, lines 37-40)

Gannett does not teach or suggest condensing the tags, much less by means of a remapping.

Some embodiments of the present innovations, for example of Claim 1 by contrast, condense a tag by re-encoding the mip mapping addresses to a length which is only one bit longer than the max condensed length of x and y addresses. For example:

> Thus, in this sample embodiment, the tag length derived from (i, j, map) inputs is reduced (e.g. from 28 to 23) by:
>
> splitting odd/even maps into two banks (already done for other reasons (viz.: 1. for mip mapping with high quality, we are always accessing texels from both an even level and an odd level; and 2. for applying more than one texture map, the two separate maps are referenced separately);
>
> ignoring least significant bits of i and of j, due to the use of 2x2 patches; and
>
> getting two or more bits from a remapping, which exploits the different address resolutions implied by level of detail settings in the different mip mapping processes to re-encode the mip mapping addresses into a length which is only one bit longer than the max condensed length of x and y addresses. (page 10, lines 23-33)

Gannett does not teach or suggest any of the above cited steps for condensing tags by means of a remapping. (Of course, this text in the specification is not intended to limit the scope of

the claims. It is cited only as an example to explain one embodiment of the present inventions.)

The Examiner has suggested that col. 19, lines 37-40; col. 35, lines 47-64; and Fig. 18 of *Gannett* teaches this element. However, Applicant respectfully disagrees with this suggestion. Col. 19, lines 37-40 of *Gannett* states:

> *The tags are 23-bit fields that include eight bits representing the texture ID of the texture data, a bit used in determining the map number of the texture data, and the seven high-order S and T coordinates of the texture data.*

As stated earlier, this section of *Gannett* merely states that it creates 23-bit tags. Creating a 23-bit tag does not teach or suggest condensing a tag by re-encoding the mip mapping addresses.

Col. 35, lines 47-64 of *Gannett* states:

> *It should be understood that maps smaller than the maximum 32KX32K do not employ the full S and T address fields, such that the smaller the map, the more high-order S and T address bits that are unused. As shown in FIG. 18, for maps having a map number greater than eight, the block tag bit corresponding to the least significant unused T coordinate bit is set to logical "0", and the block tag bits corresponding to the remaining high-order T coordinate bits and the map bit are set to logical "1". For map number fifteen, which uses all of the T coordinate bits, the map bit is set to logical "0". By reading block tag bits [14:07] that correspond to the map bit and the high-order T coordinate bits [14:8], the position of the first logical "0" encountered reading left to right indicates the map number represented by the block tag. If a logical 1 is included in all of block tag bits [14:08], then map numbers eight and less are represented.*

This section of *Gannett* merely teaches using a "0", in the first logical position encountered when reading the tag from left to right, to indicate the map number represented by the block tag. Fig. 18 of *Gannett* merely illustrates the placement of the "0". This does not in any way condense the 23-bit tag taught by *Gannett*.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference,

arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990).

Accordingly, Claim 1 is not anticipated by *Gannett*.

Claim 3

> A graphics processing method, comprising caching texture memory fetches using a cache tag assignment in which a unique relation between a mip-mapping-level-of-detail parameter and coordinate bits defines a smaller tag address for any given memory address.

Again, the Examiner has suggested that col. 19, lines 37-40 of *Gannett* teaches each and every element of this claim. As stated earlier, however, this section of *Gannett* merely states that it creates 23-bit tags. This section does not teach, "using a cache tag assignment in which a unique relation between a mip-mapping-level-of-detail parameter and coordinate bits defines a smaller tag address for any given memory address." *Gannett* only discloses a 23-bit tag. It does not disclose generating tags of a size smaller than 23 bits.

The Examiner has also suggested that col. 35, lines 47-64 of *Gannett* teaches this element. This section of *Gannett*, however, merely teaches using a "0", in the first logical position encountered when reading the tag from left to right, to indicate the map number represented by the block tag. Fig. 18 of *Gannett* merely illustrates the placement of the "0". This does not in any way condense the 23-bit tag taught by *Gannett*.

Accordingly, Claim 3 is not anticipated by *Gannett*.

2. *Gannett* does not teach or suggest generating lookup tags that require m+n-1 or fewer bits.

Claim 7

> A cache system for a texture map, comprising:
>
> a texture memory containing at least one map, wherein addresses for said map can require m bits for an x-axis coordinate, n bits for a y-axis coordinate, and p bits for a map-level identifier; and
>
> a direct-mapped texture cache for said texture memory, configured to be accessed using lookup tags which require m + n - 1 or fewer bits.

As discussed above, Claim 7 recites features not taught or suggested by *Gannett*. Specifically, Claim 7 recites, "a direct-mapped texture cache for said texture memory, configured to be accessed using lookup tags which require m + n - 1 or fewer bits."

The Examiner has suggested that col. 19, lines 34-64 of *Gannett* teaches this element of Claim 7. However, Applicant respectfully disagrees with this suggestion. This section of *Gannett* states:

> *During rendering, the tiler/boundary checker 72 generates a read cache tag for the block of texture data that maps to the pixel to be rendered. The manner in which the cache block tag and the read cache tag are generated is explained in more detail below. The tags are 23-bit fields that include eight bits representing the texture ID of the texture data, a bit used in determining the map number of the texture data, and the seven high-order S and T coordinates of the texture data. The cache directory 78 compares the read cache tag provided from the tiler/boundary with the block tags stored in the directory to determine whether the block of texture data to be used in rendering is in the cache memory. If the block tag of the texture data that maps to the primitive to be rendered is stored in (i.e., hits) the cache directory, then the cache directory generates a block index that indicates the physical location of the block of texture data in the cache that corresponds to the hit tag. The computation of the block index is discussed in greater detail below. A texel address is also generated by the tiler/boundary checker 72 for each texel to be read from the cache and indicates the location of the texel within the block. The texel address includes low-order address bits of the interpolated S,T coordinates for larger size maps, and is computed based on an algorithm described below for smaller size maps. The block index and texel address together comprise the cache address which indicates the location of the texel within the cache. As is described in greater detail below, the LSBs of the S and T coordinates are decoded to determine in which of four cache interleaves the texel is stored, and the remaining bits of the cache address are provided to the texel cache access circuit 82 along with a command over line 84 to read the texel data stored at the addressed location in the cache.*

The above cited section of *Gannett* teaches generating a cache address to indicate the location of a texel within a cache by combining the texel's address with the block index. It does not teach or disclose generating a lookup tag that require m + n - 1 or fewer bits. The 23-bit tag disclosed by *Gannett* consists of eight bits representing the texture ID of the texture data, a bit used in determining the map number of the texture data, and the seven high-order S and T coordinates of the texture data. Since m and n represent x and y

coordinate bits, *Gannett* would have to teach or disclose condensing its 23-bit tag into a condensed tag of 13 bits (7 + 7 - 1) in order to teach or disclose this element of Claim 7. Clearly, it does not.

Accordingly, Claim 7 is not anticipated by *Gannett*.

Claim 8

> A graphics processing method, comprising the steps of:
> (a.) caching texture memory fetches, using a cache tag assignment which is essentially unique mapped, while
> (b.) generating condensed cache tags, by means of a remapping which exploits different address resolutions implied by level of detail settings in different mip mapping processes to re-encode mip mapping addresses into a length which is only one bit longer than a maximum condensed length of a spatial address
> (c.) and using said condensed tags for said caching step (a.).

Claim 8 recites features not taught or suggested by *Gannett*. Specifically, Claim 7 recites, "generating condensed cache tags, by means of a remapping which exploits different address resolutions implied by level of detail settings in different mip mapping processes to re-encode mip mapping addresses into a length which is only one bit longer than a maximum condensed length of a spatial address."

3. *Gannett* does not teach or suggest generating condensed tags, much less condensed tags which are only one bit longer than a maximum condensed length of a spatial address.

The Examiner has suggested that col. 19, lines 37-40 of *Gannett* discloses this element of Claim 8. However, Applicant respectfully disagrees with this suggestion.

Again, as stated earlier, this section of *Gannett* merely states that it creates 23-bit tags. Creating a 23-bit tag is not the same thing as condensing a tag by re-encoding the mip mapping addresses into a length that is only one bit longer than the maximum condensed length of a spatial address. As stated earlier, *Gannett* teaches a tag whose spatial address has a maximum condensed length of 14 bits (7 + 7). Therefore, in order for *Gannett* to teach or disclose this element of Claim 8, it would have to teach or disclose condensing its 23-bit tag into a 15-bit tag (7 +7 + 1). Clearly, it does not.

Accordingly, Claim 8 is not anticipated by *Gannett*.

Finally, dependent Claims 4 and 5, which depend directly from independent Claim 3 and incorporate all the limitations thereof, also include additional limitations that are not shown or suggested by *Gannett*.

Specifically, Claim 4 recites, "The graphics processing method of Claim 3, wherein said cache tag assignment is generated by combining a mip-map-level-of-detail parameter which can have at least $2^{J-1} + 1$ different values together with coordinate bits which can have as many as 2^K different values into fewer than J + 2K bits without loss of information; wherein J represents the number of bits for a level of detail and K represents the number of bits for arbitrary coordinate values."

The Examiner has suggested with regard to this claim that, "Gannett discloses 23 bits for a tag in col. 19 lines 37-40 that is less than 26 bits." Applicant agrees with the Examiner's suggestion that *Gannett* discloses a 23-bit tag. However, Applicant does not agree with the Examiner's suggestion that Claim 4 discloses a 26-bit tag. As stated earlier, the 23-bit tag disclosed by *Gannett* consists of eight bits representing the texture ID of the texture data, a bit used in determining the map number of the texture data, and the seven high-order S and T coordinates of the texture data. Since J represents the number of bits for a level of detail (1 bit) and K represents the number of bits for arbitrary coordinate values (7 bits), *Gannett* would have to teach or disclose condensing its 23-bit tag into a condensed tag of fewer than 15 bits (1 + 2(7)) in order to teach or disclose this element of Claim 4. Clearly, it does not.

Claim 5 recites, "The graphics processing method of Claim 3, wherein said cache tag assignment is generated by combining a first parameter which can have at least $2^{J-1} + 1$ different values together with coordinate bits which can have as many as 2^K different values into fewer than J + 2K bits without loss of information; wherein said first parameter and said coordinate bits are three-dimensional coordinates; and wherein J represents the number of bits for a level of detail and K represents the number of bits for arbitrary coordinate values."

The Examiner has suggested with regard to this claim that col. 19, lines 37-40 and col. 13, lines 62-67 of *Gannett* discloses each and every element of this claim. However,

Applicant respectfully disagrees with this suggestion. Again, as stated earlier, col. 19, lines 37-40 of *Gannett* merely discloses creating 23-bit tags. Col. 13, lines 62-67 of *Gannett* states:

> *The data representing the triangle primitives includes the x,y,z object ptxel coordinates for at least one vertex, the object color R,G,B values of the at least one vertex, the coordinates in S,T of the portions of the texture map that correspond to the at least one vertex, and the plane equation of the triangle.*

This section of *Gannett* clearly does not teach or disclose condensing a cache tag into fewer than J + 2K bits. Again, as stated earlier, the 23-bit tag disclosed by *Gannett* consists of eight bits representing the texture ID of the texture data, a bit used in determining the map number of the texture data, and the seven high-order S and T coordinates of the texture data. Since J represents the number of bits for a level of detail (1 bit) and K represents the number of bits for arbitrary coordinate values (7 bits), *Gannett* would have to teach or disclose condensing its 23-bit tag into a condensed tag of fewer than 15 bits (1 + 2(7)) in order to teach or disclose this element of Claim 5. Clearly, it does not.

Thus, for the reasons discussed above, Applicant respectfully requests withdrawal of this rejection.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or Patrick C.R. Holmes for an interview to resolve any remaining issues.

Respectfully submitted,

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